Fig. 1 PRIOR ART

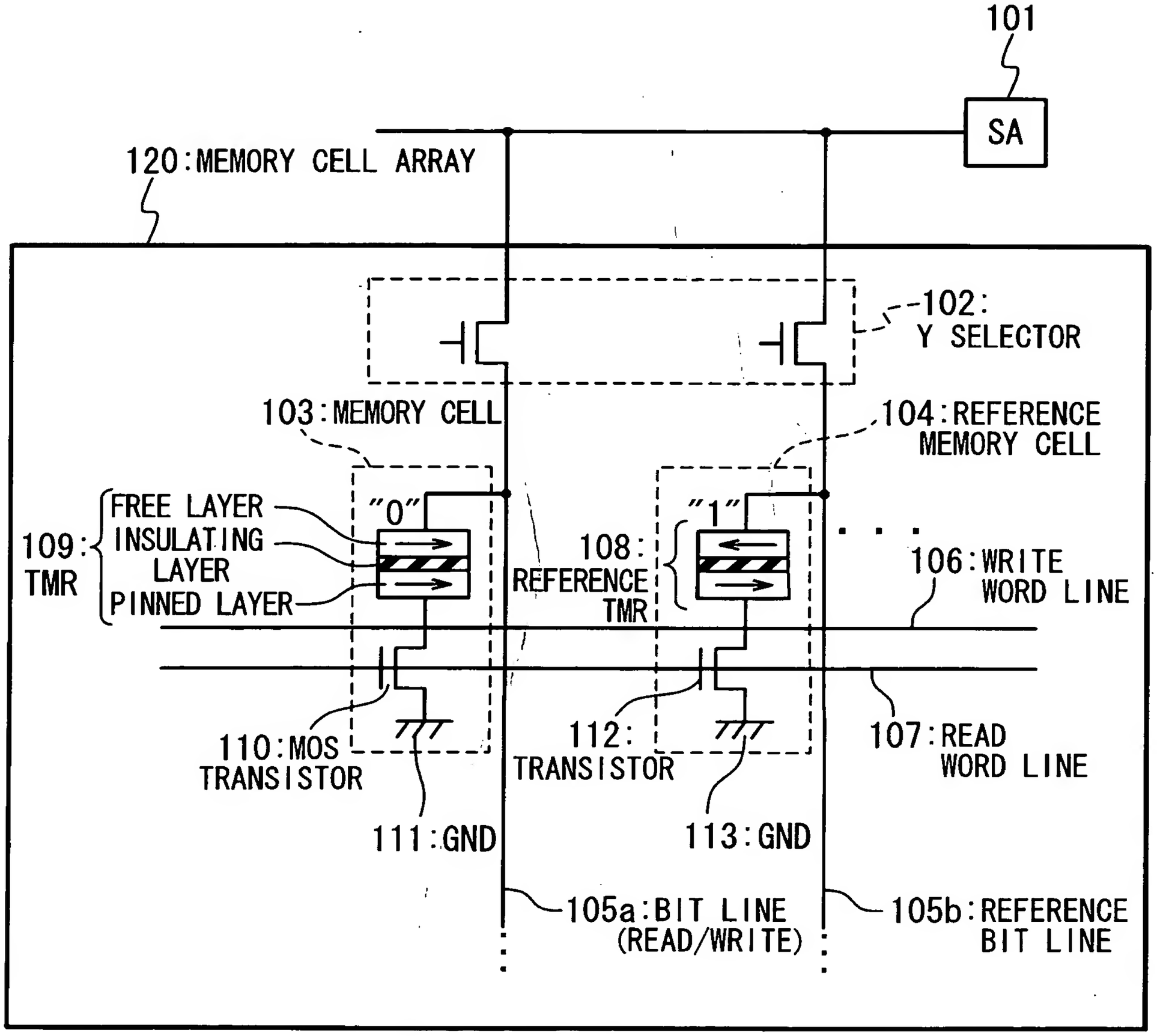


Fig. 2 PRIOR ART

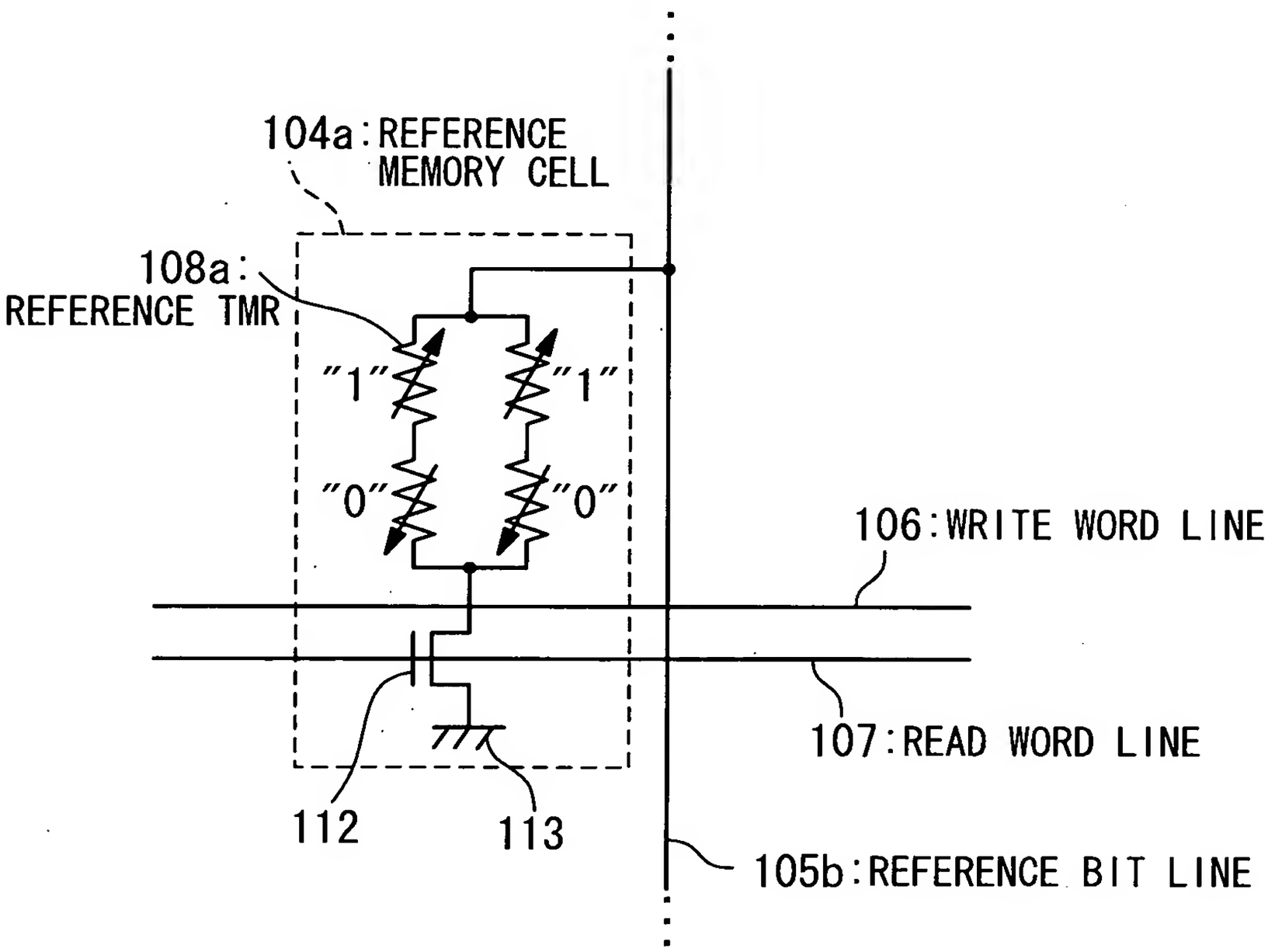


Fig. 3 PRIOR ART

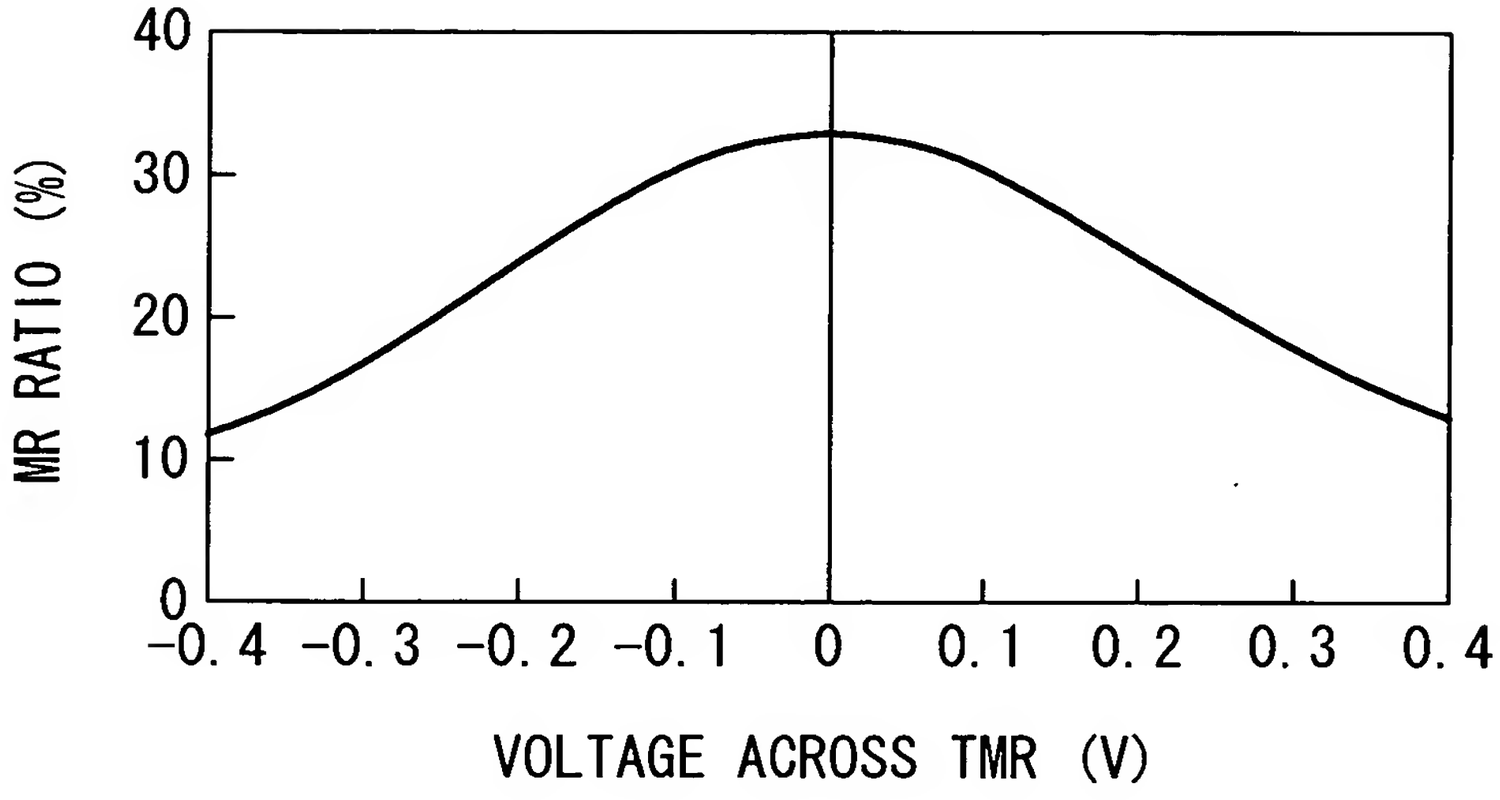


Fig. 4

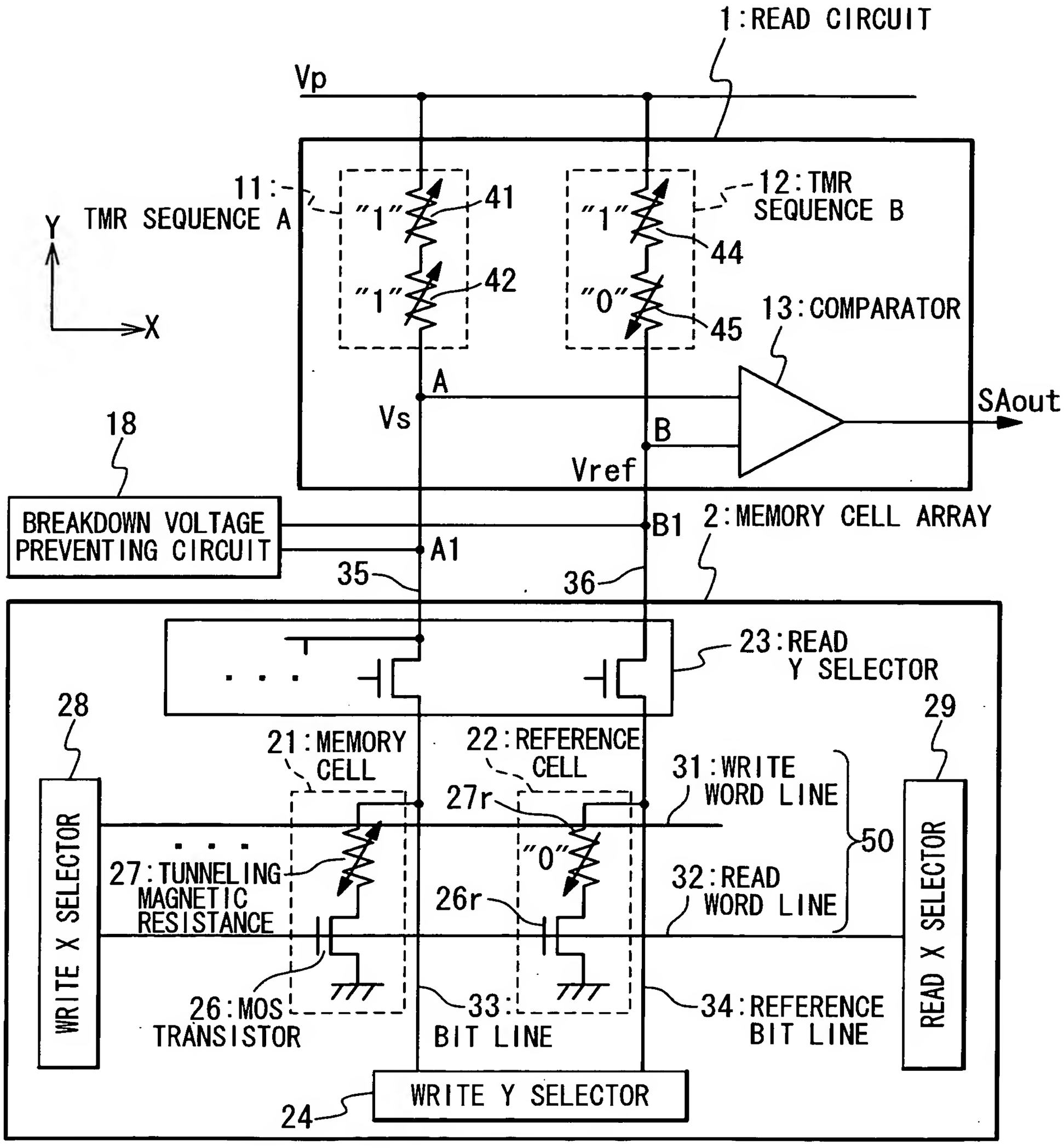

1:READ CIRCUIT
Vp
11:
TMR SEQUENCE A
"1"
41
"1"
42
12:TMR
SEQUENCE B
"1"
44
"0"
45
13:COMPARATOR
Y
X
A
Vs
B
Vref
SAout
18
BREAKDOWN VOLTAGE
PREVENTING CIRCUIT
A1
B1
35
36
2:MEMORY CELL ARRAY
23:READ
Y SELECTOR
28
29
21:MEMORY
CELL
22:REFERENCE
CELL
31:WRITE
WORD LINE
27r
"0"
50
27:TUNNELING
MAGNETIC
RESISTANCE
26r
32:READ
WORD LINE
WRITE X SELECTOR
READ X SELECTOR
26:MOS
TRANSISTOR
33:
BIT LINE
34:REFERENCE
BIT LINE
WRITE Y SELECTOR
24

Fig. 5A

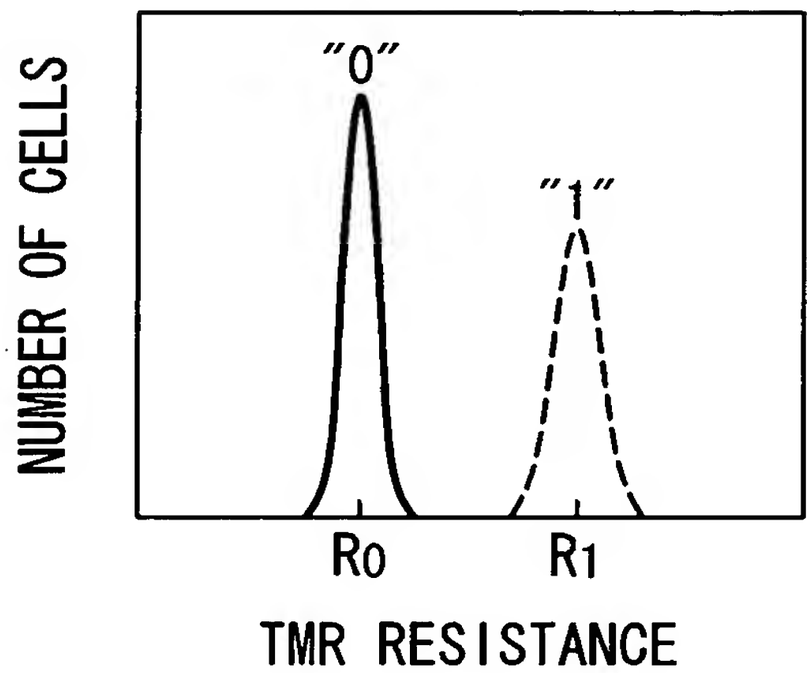


Fig. 5B

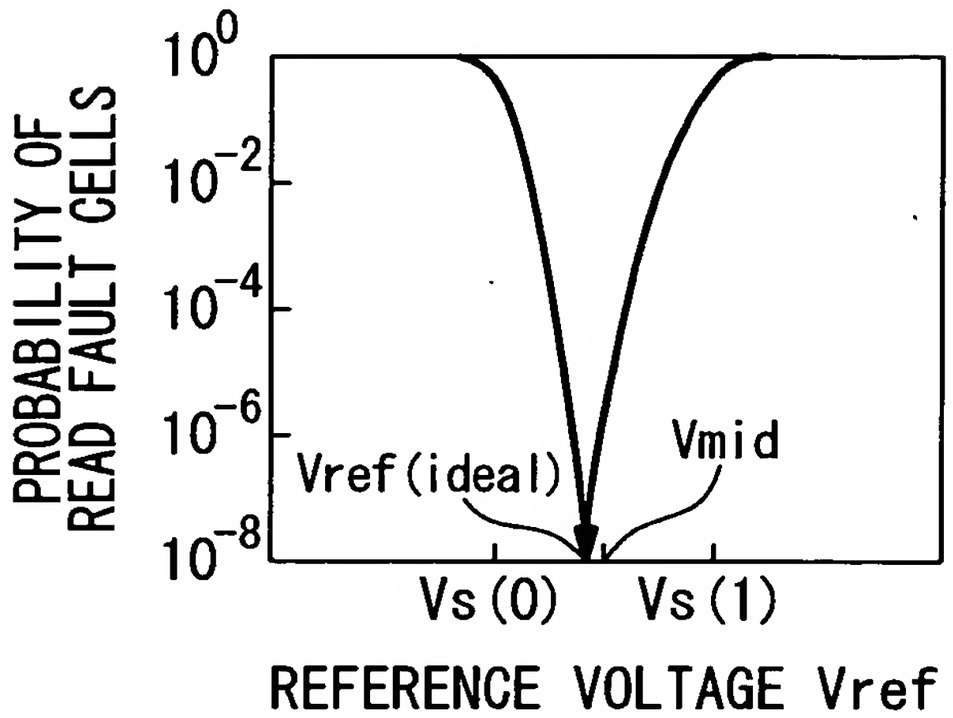


Fig. 6

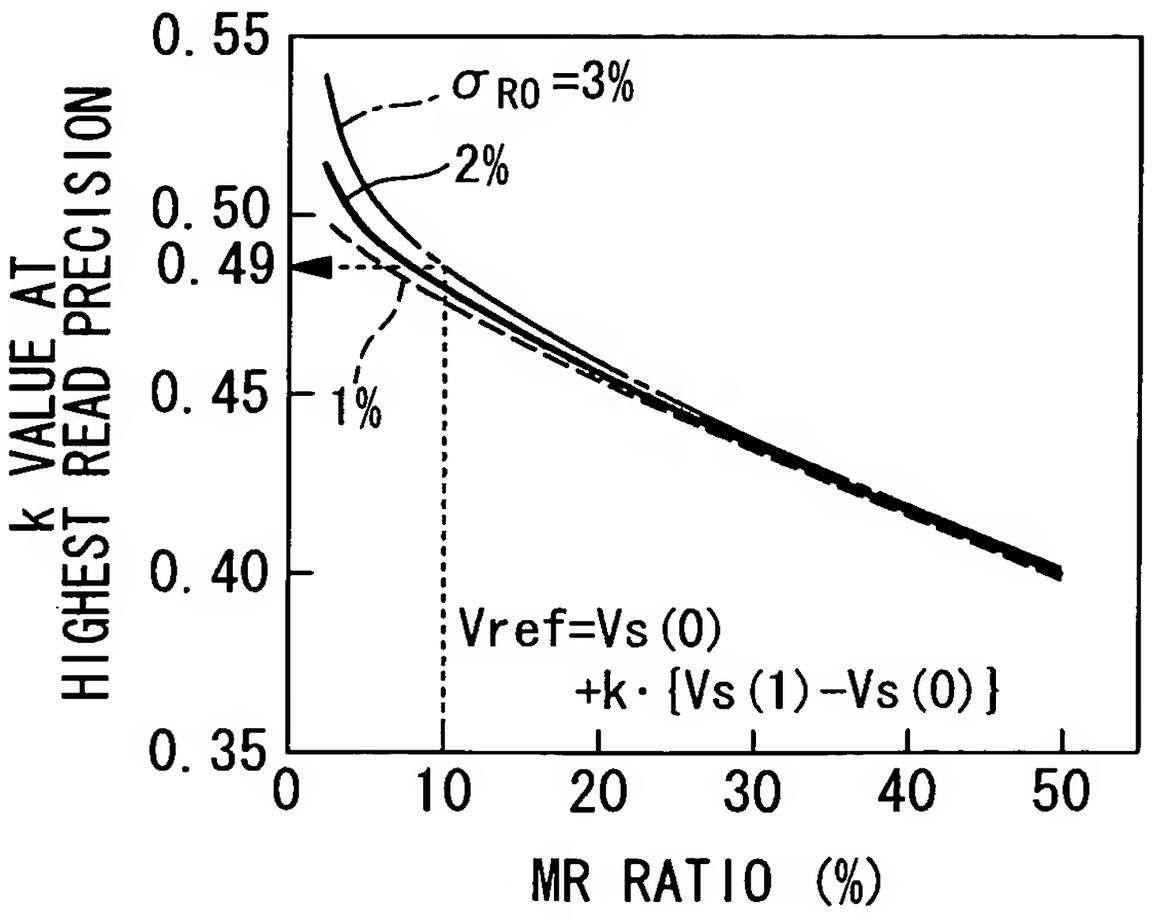


Fig. 7

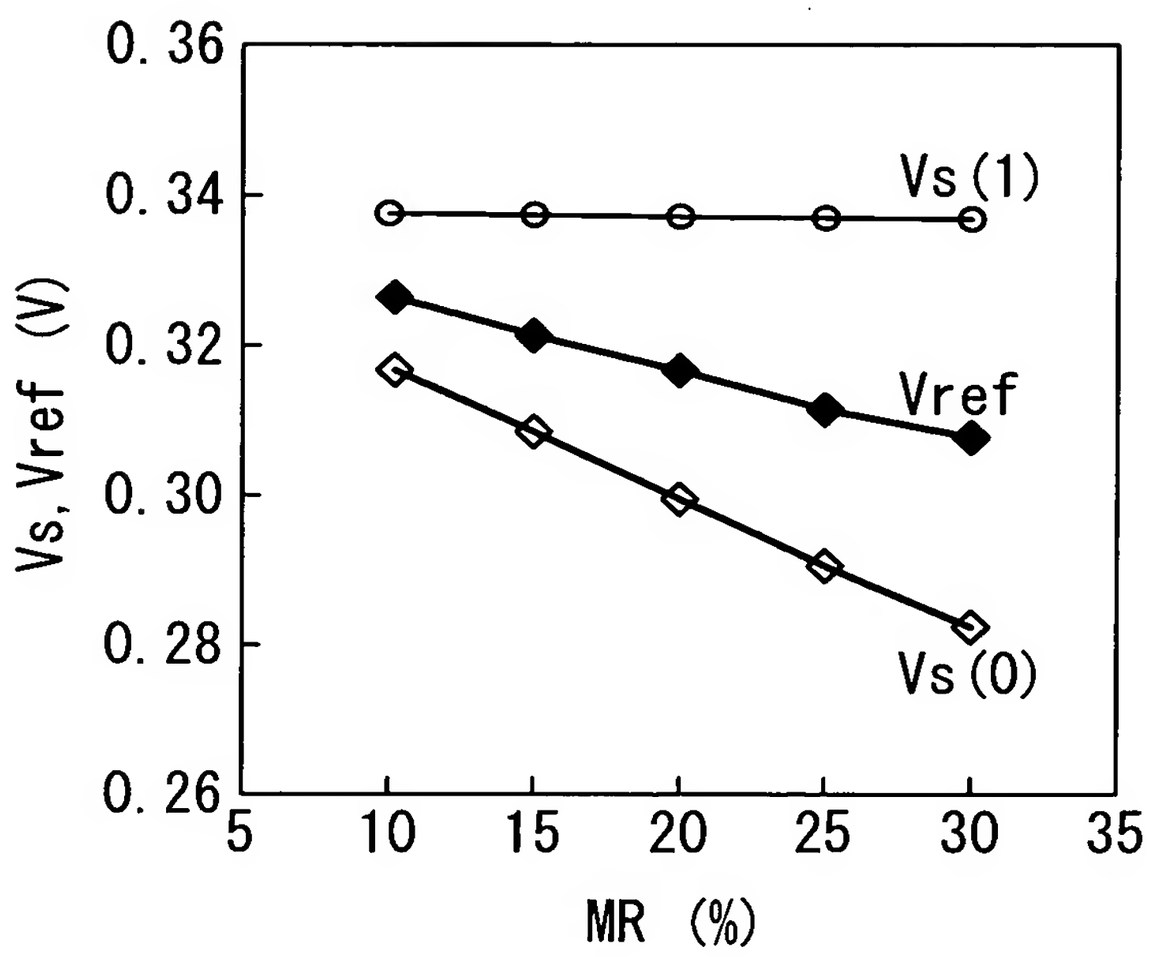

0.36
0.34
0.32
0.30
0.28
0.26
Vs, Vref (V)
Vs(1)
Vref
Vs(0)
5
10
15
20
25
30
35
MR (%)

Fig. 8

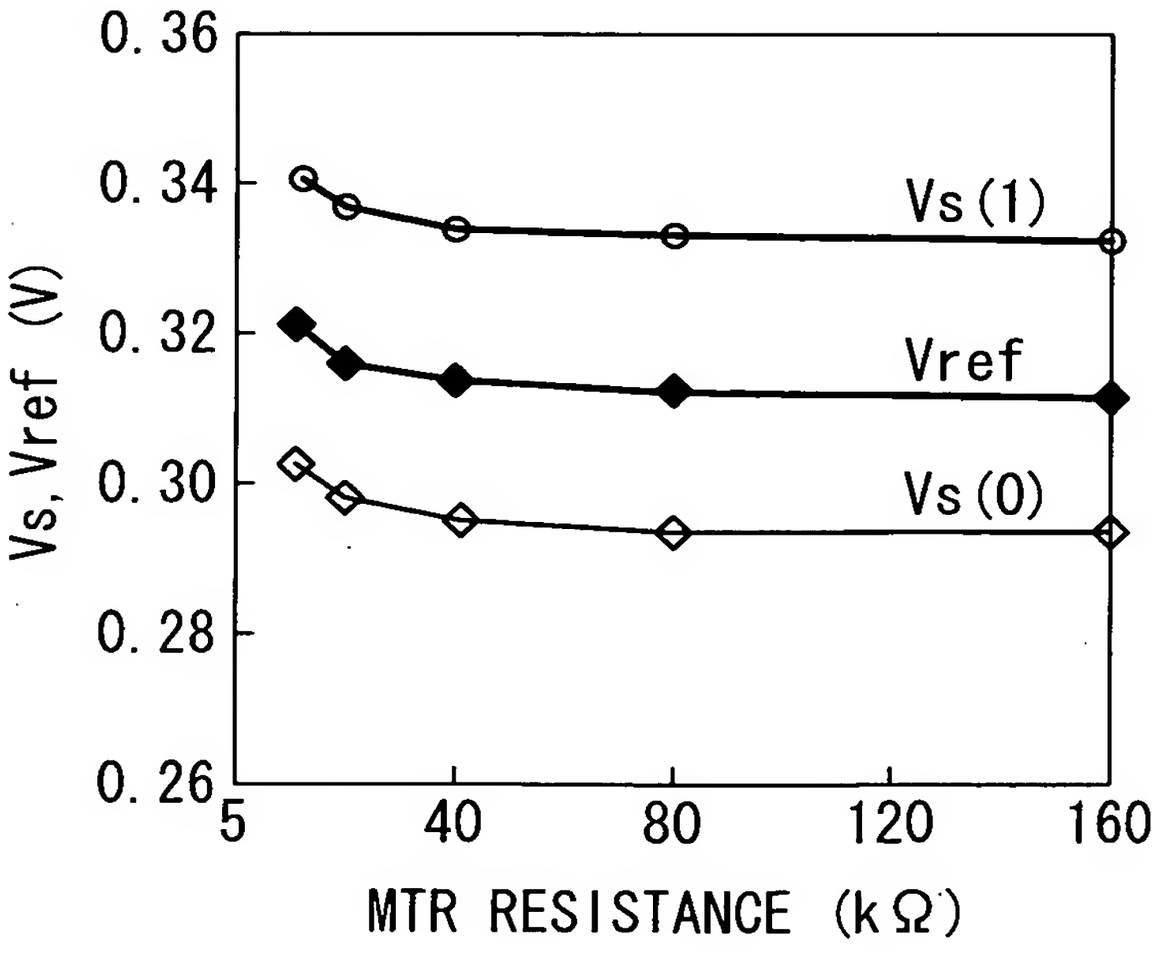

0.36
0.34
0.32
0.30
0.28
0.26
Vs, Vref (V)
Vs(1)
Vref
Vs(0)
5
40
80
120
160
MTR RESISTANCE (kΩ)

Fig. 9

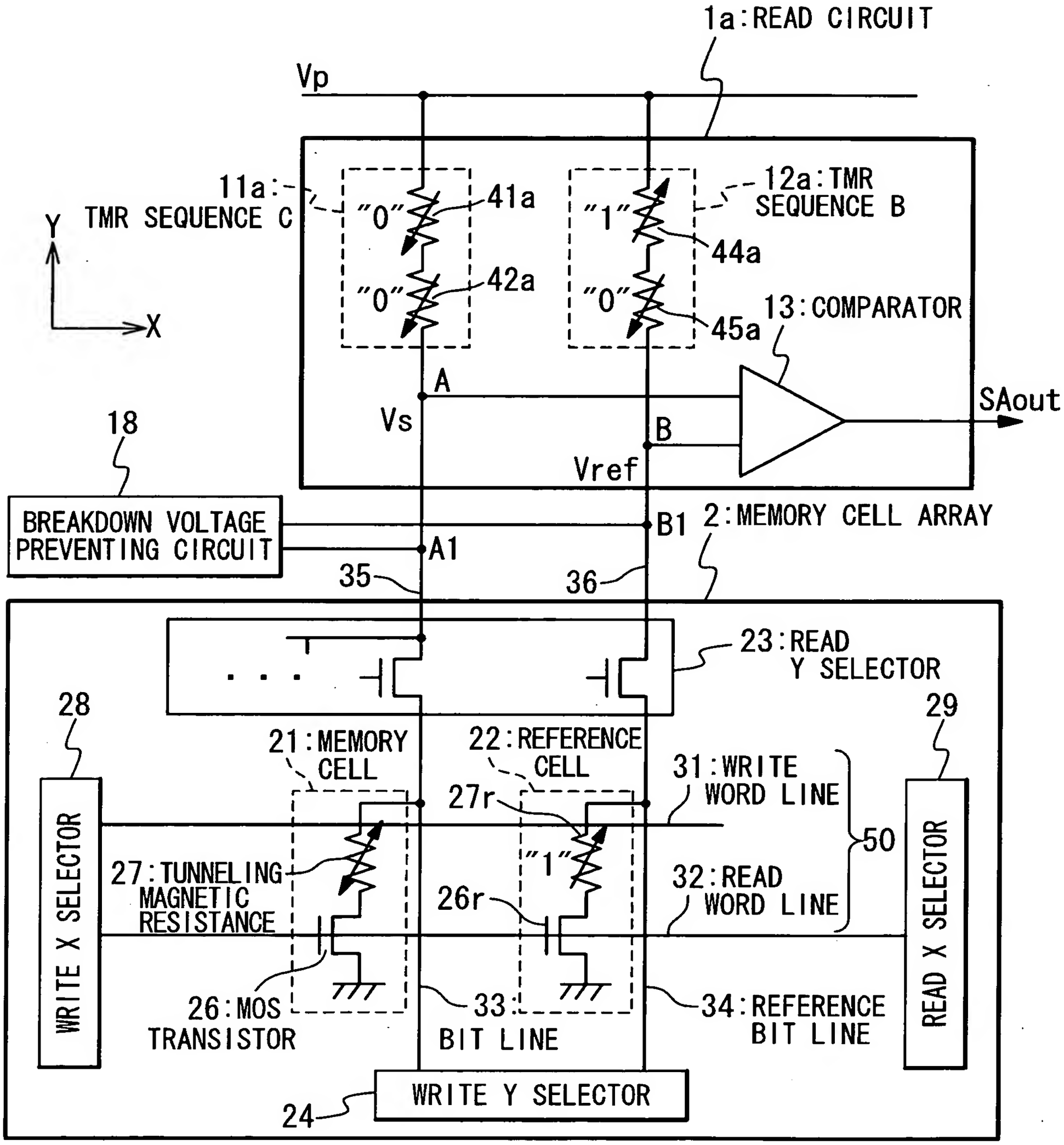

1a:READ CIRCUIT
Vp
11a:
TMR SEQUENCE C
"0"
41a
"0"
42a
12a:TMR
SEQUENCE B
"1"
44a
"0"
45a
13:COMPARATOR
Y
X
A
Vs
B
Vref
SAout
18
BREAKDOWN VOLTAGE
PREVENTING CIRCUIT
A1
B1
2:MEMORY CELL ARRAY
35
36
23:READ
Y SELECTOR
28
29
21:MEMORY
CELL
22:REFERENCE
CELL
31:WRITE
WORD LINE
27r
50
WRITE X SELECTOR
READ X SELECTOR
27:TUNNELING
MAGNETIC
RESISTANCE
"1"
32:READ
WORD LINE
26r
26:MOS
TRANSISTOR
33:
BIT LINE
34:REFERENCE
BIT LINE
WRITE Y SELECTOR
24

Fig. 10

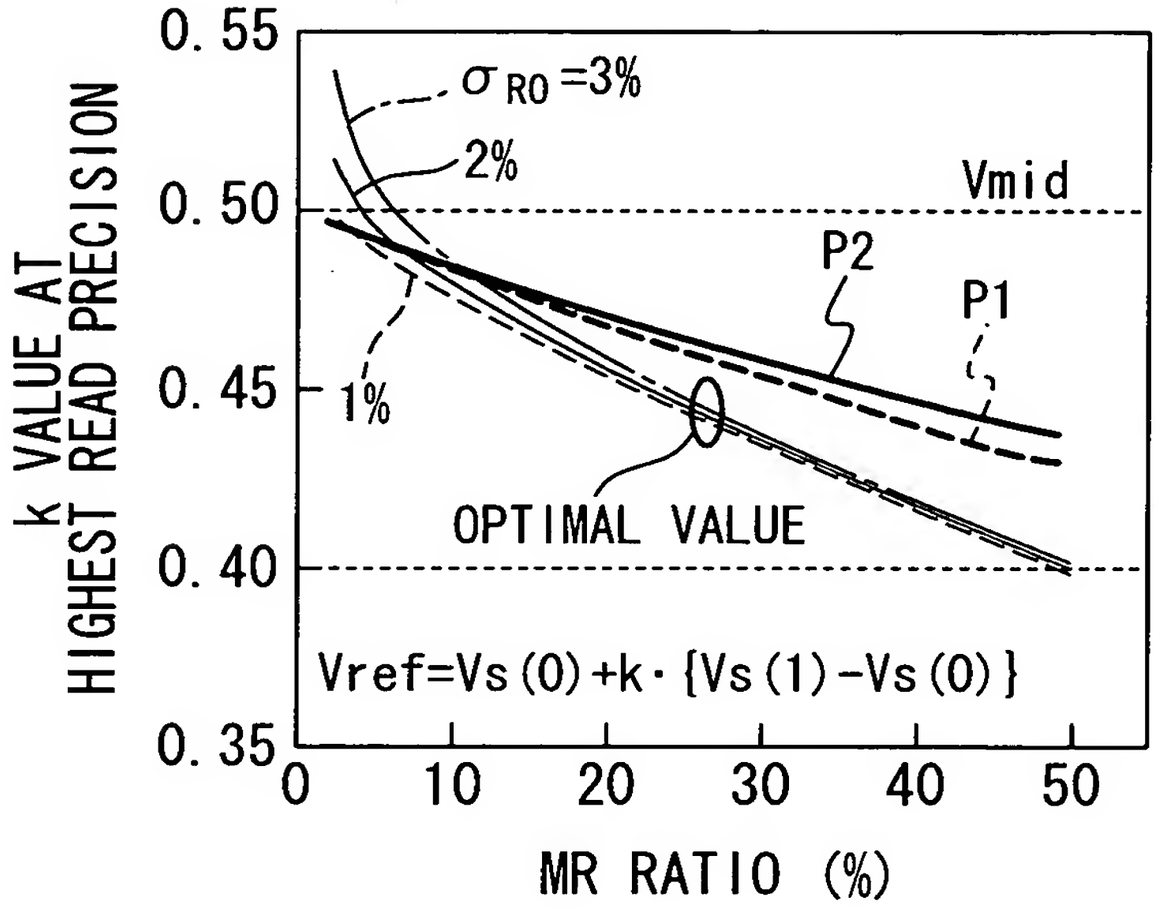

k VALUE AT HIGHEST READ PRECISION
0.55
0.50
0.45
0.40
0.35
σRO=3%
2%
1%
Vmid
P2
P1
OPTIMAL VALUE
Vref=Vs(0)+k·{Vs(1)-Vs(0)}
0
10
20
30
40
50
MR RATIO (%)

Fig. 11

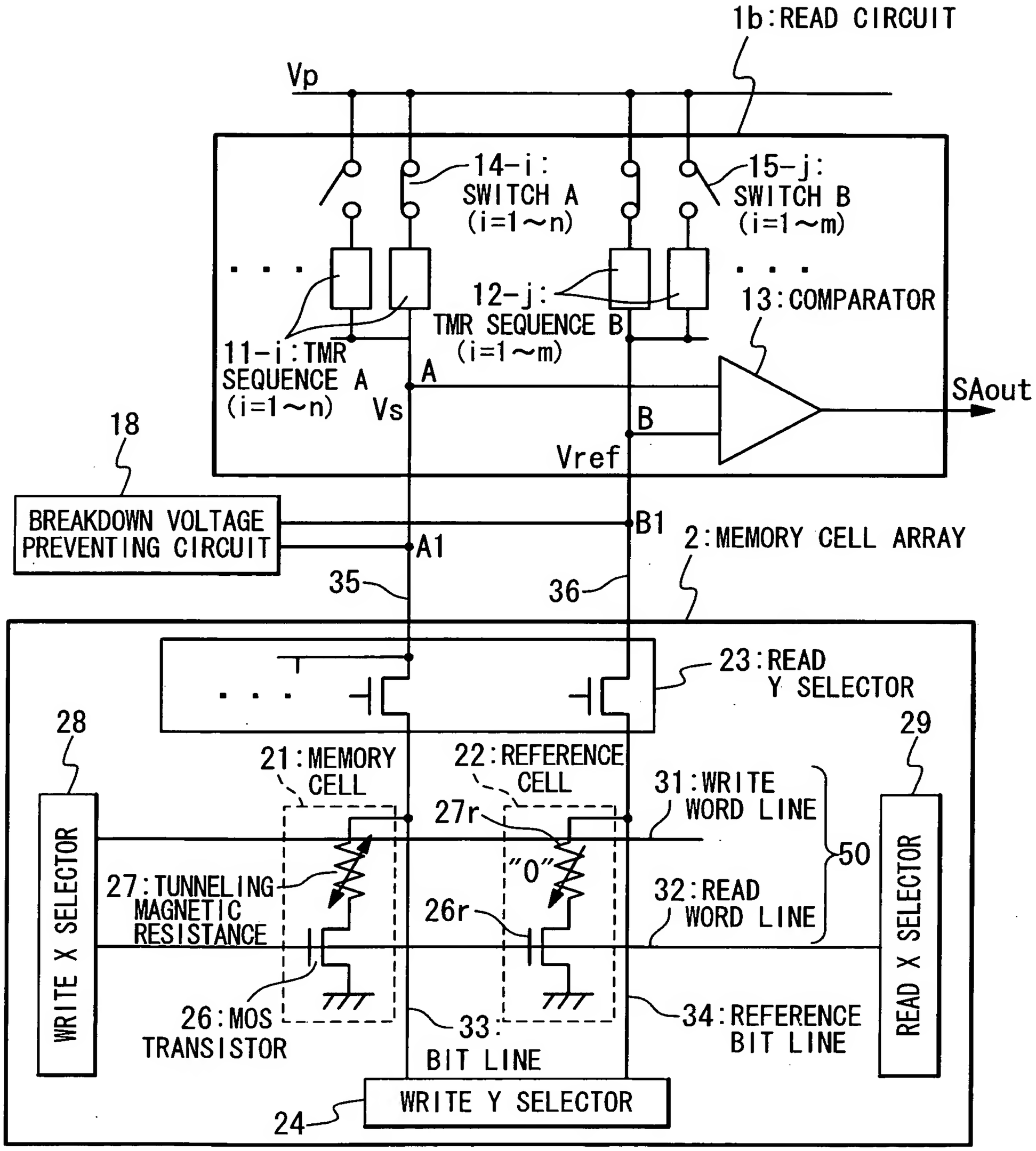
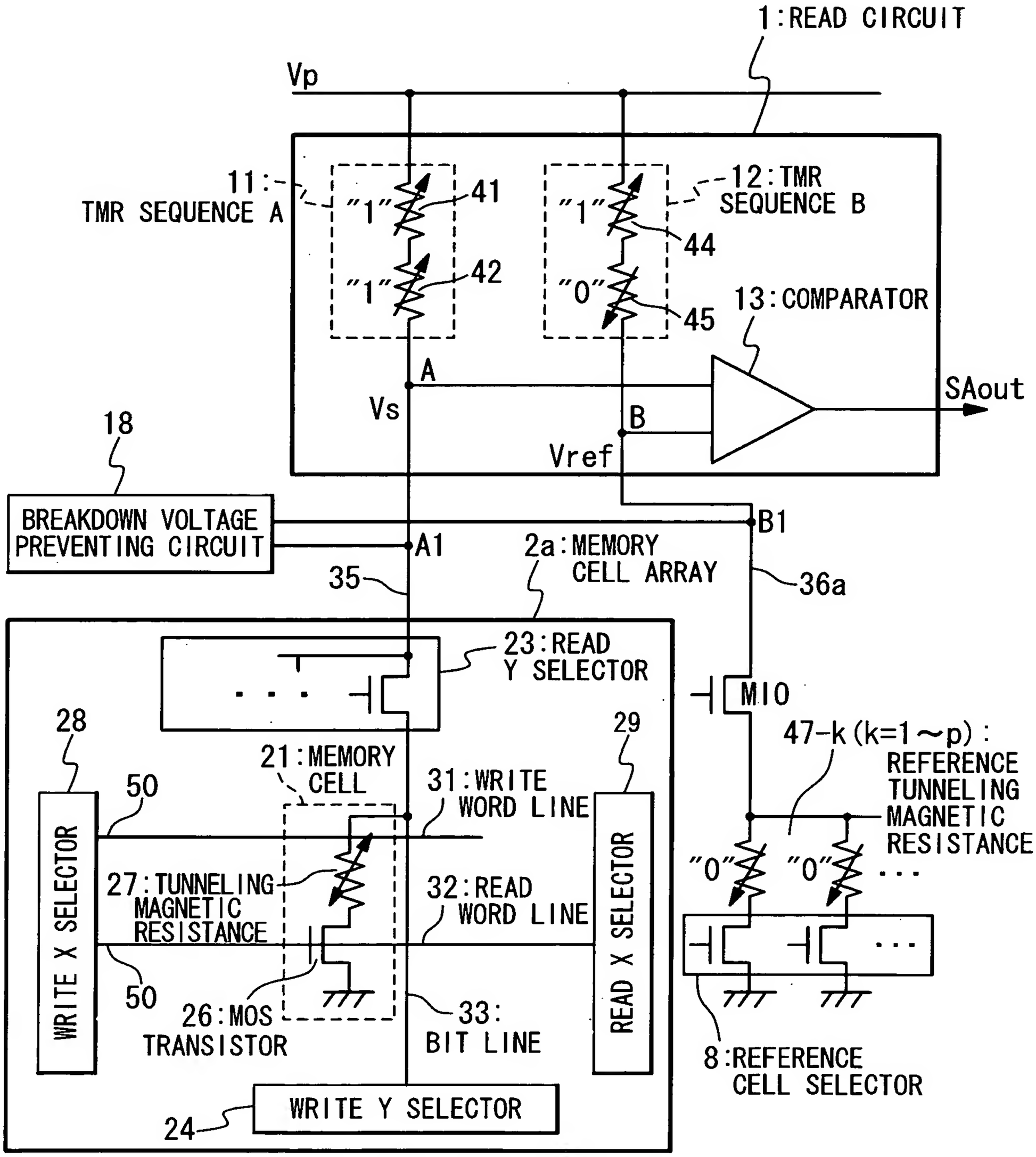

1b:READ CIRCUIT
Vp
14-i:
SWITCH A
(i=1～n)
15-j:
SWITCH B
(i=1～m)
12-j:
TMR SEQUENCE B
(i=1～m)
13:COMPARATOR
11-i:TMR
SEQUENCE A
(i=1～n)
A
Vs
B
Vref
SAout
18
BREAKDOWN VOLTAGE
PREVENTING CIRCUIT
A1
B1
2:MEMORY CELL ARRAY
35
36
23:READ
Y SELECTOR
28
29
21:MEMORY
CELL
22:REFERENCE
CELL
31:WRITE
WORD LINE
27r
"0"
50
27:TUNNELING
MAGNETIC
RESISTANCE
32:READ
WORD LINE
26r
WRITE X SELECTOR
READ X SELECTOR
26:MOS
TRANSISTOR
33:
BIT LINE
34:REFERENCE
BIT LINE
WRITE Y SELECTOR
24

Fig. 12


1:READ CIRCUIT
Vp
11:
TMR SEQUENCE A
"1"
41
"1"
42
12:TMR
SEQUENCE B
"1"
44
"0"
45
13:COMPARATOR
A
Vs
B
Vref
SAout
18
BREAKDOWN VOLTAGE
PREVENTING CIRCUIT
A1
B1
2a:MEMORY
CELL ARRAY
35
36a
23:READ
Y SELECTOR
MIO
28
29
21:MEMORY
CELL
50
31:WRITE
WORD LINE
27:TUNNELING
MAGNETIC
RESISTANCE
32:READ
WORD LINE
50
26:MOS
TRANSISTOR
33:
BIT LINE
WRITE X SELECTOR
READ X SELECTOR
WRITE Y SELECTOR
24
47-k (k=1~p):
REFERENCE
TUNNELING
MAGNETIC
RESISTANCE
"0"
"0"
8:REFERENCE
CELL SELECTOR

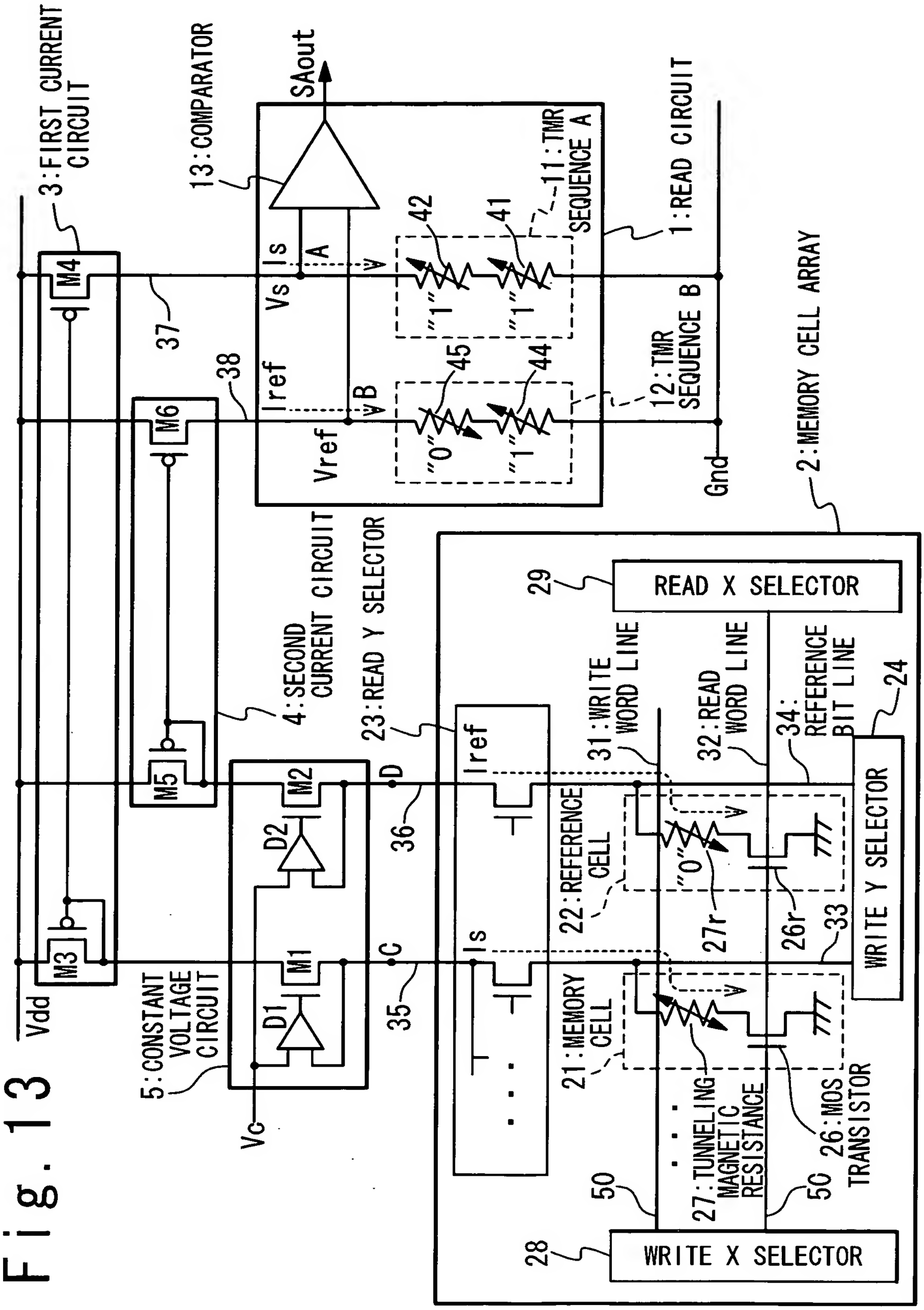

1:READ CIRCUIT
2:MEMORY CELL ARRAY
3:FIRST CURRENT CIRCUIT
4:SECOND CURRENT CIRCUIT
5:CONSTANT VOLTAGE CIRCUIT
11:TMR SEQUENCE A
12:TMR SEQUENCE B
13:COMPARATOR
21:MEMORY CELL
22:REFERENCE CELL
23:READ Y SELECTOR
24
26:MOS TRANSISTOR
26r
27:TUNNELING MAGNETIC RESISTANCE
27r
28
29
31:WRITE WORD LINE
32:READ WORD LINE
33
34: REFERENCE BIT LINE
35
36
37
38
41
42
44
45
50
50
777
A
B
C
D
Gnd
Is
Iref
Iref
Iref
SAout
Vc
Vdd
Vref
Vs
WRITE X SELECTOR
WRITE Y SELECTOR
READ X SELECTOR
M1
M2
M3
M4
M5
M6
D1
D2
"0"
"1"
"1"
"1"
"0"
"0"

Fig. 13

Fig. 14

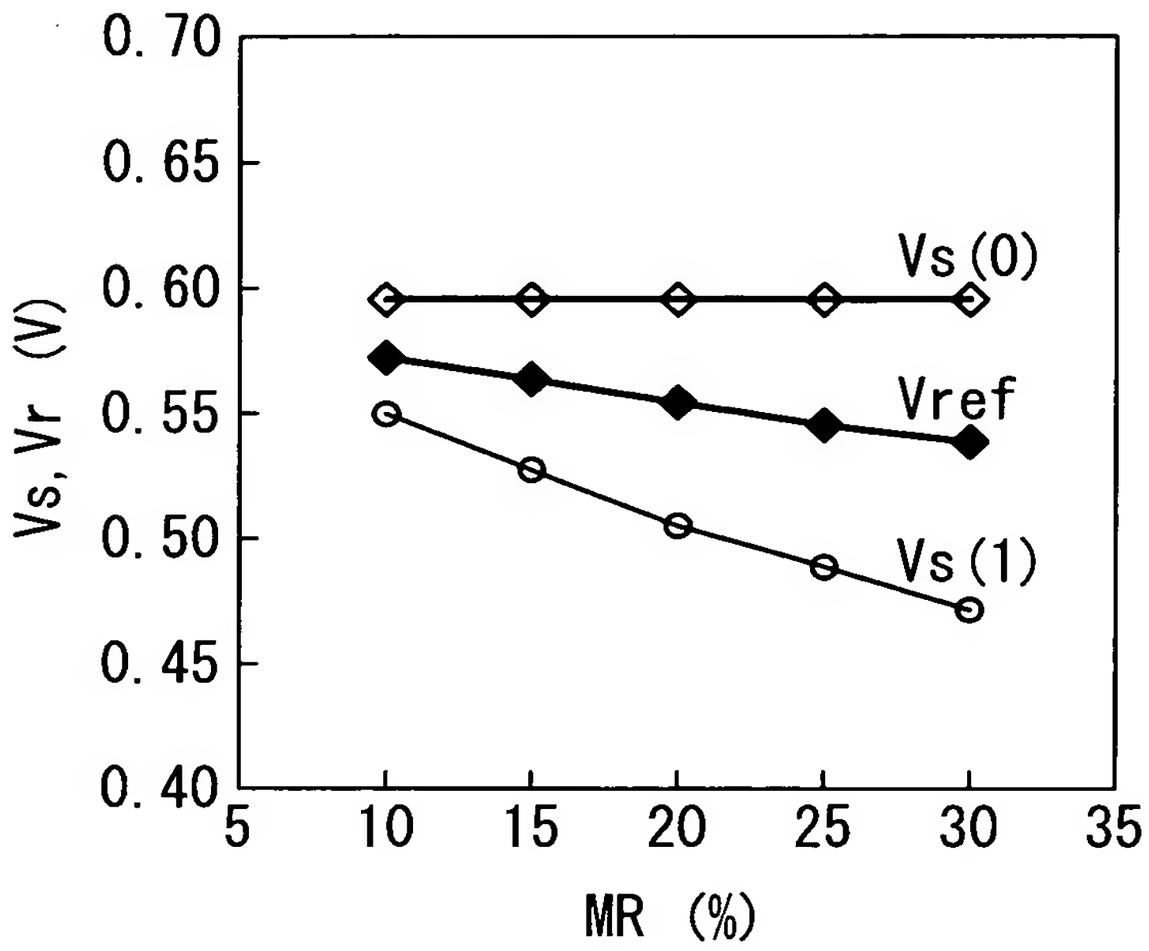

0.70
0.65
0.60
0.55
0.50
0.45
0.40
Vs, Vr (V)
Vs(0)
Vref
Vs(1)
5
10
15
20
25
30
35
MR (%)

Fig. 15

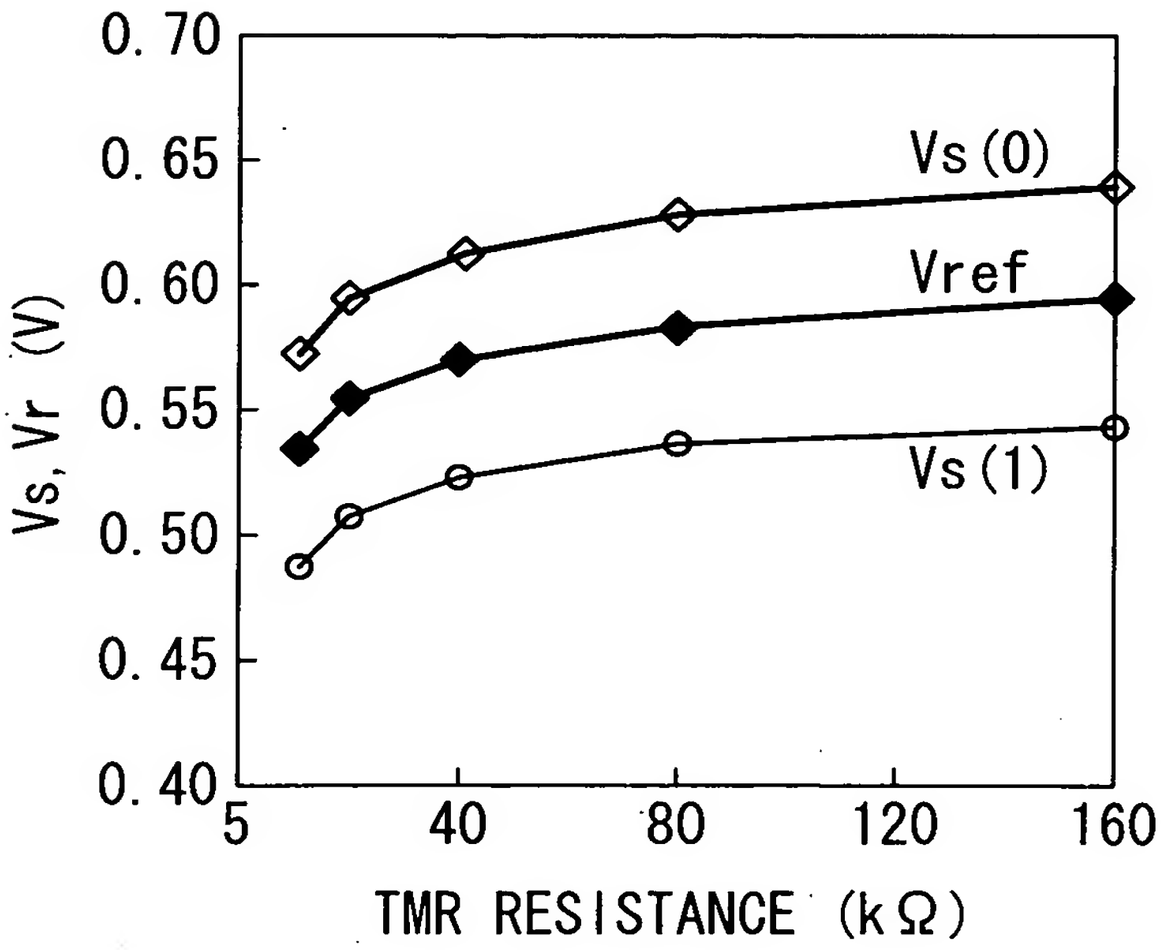
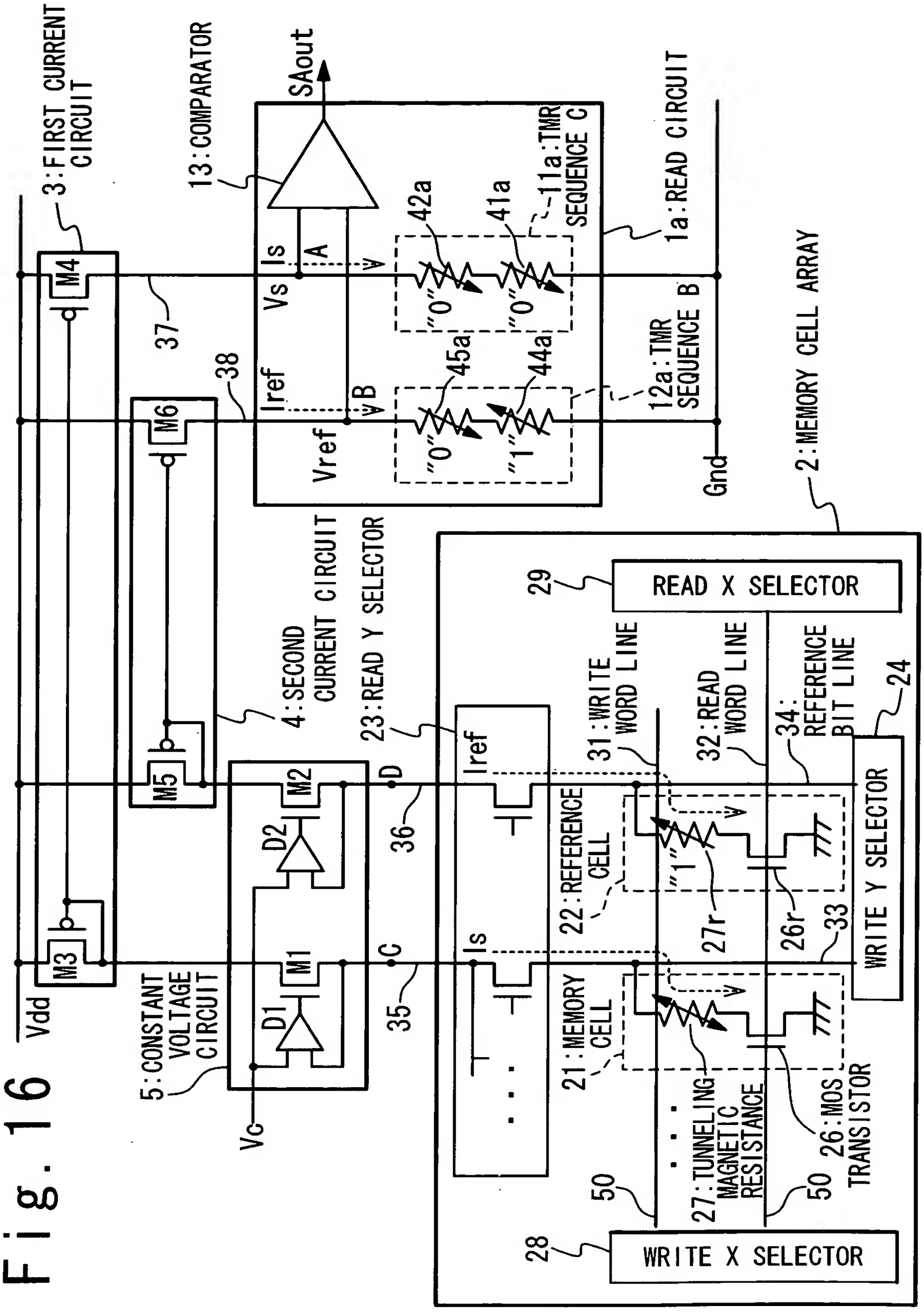
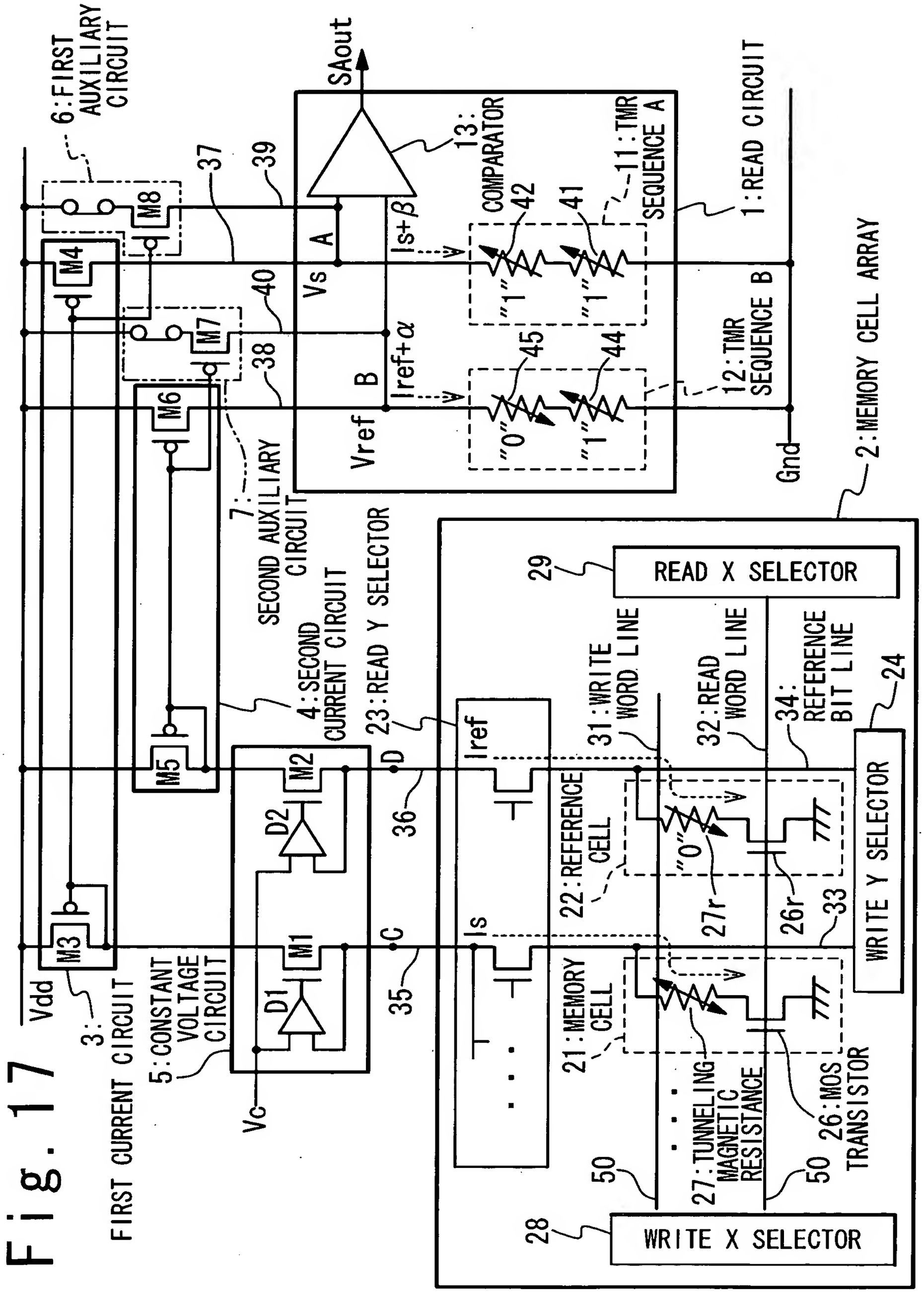

0.70
0.65
0.60
0.55
0.50
0.45
0.40
Vs, Vr (V)
Vs(0)
Vref
Vs(1)
5
40
80
120
160
TMR RESISTANCE (kΩ)

Fig. 16


3: FIRST CURRENT CIRCUIT
13: COMPARATOR
SAout
1a: READ CIRCUIT
2: MEMORY CELL ARRAY
11a: TMR SEQUENCE C
12a: TMR SEQUENCE B
42a
41a
45a
44a
Is
Iref
Vs
Vref
A
B
37
38
36
35
Gnd
Vdd
Vc
M1
M2
M3
M4
M5
M6
D1
D2
4: SECOND CURRENT CIRCUIT
5: CONSTANT VOLTAGE CIRCUIT
23: READ Y SELECTOR
29
READ X SELECTOR
31: WRITE WORD LINE
32: READ WORD LINE
34: REFERENCE BIT LINE
24
22: REFERENCE CELL
21: MEMORY CELL
27: TUNNELING MAGNETIC RESISTANCE
26: MOS TRANSISTOR
27r
26r
33
50
28
WRITE X SELECTOR
WRITE Y SELECTOR
"0"
"1"


1: READ CIRCUIT
2: MEMORY CELL ARRAY
3: FIRST CURRENT CIRCUIT
4: SECOND CURRENT CIRCUIT
5: CONSTANT VOLTAGE CIRCUIT
6: FIRST AUXILIARY CIRCUIT
7: SECOND AUXILIARY CIRCUIT
11: TMR SEQUENCE A
12: TMR SEQUENCE B
13: COMPARATOR
21: MEMORY CELL
22: REFERENCE CELL
23: READ Y SELECTOR
24: WRITE Y SELECTOR
26: MOS TRANSISTOR
27: TUNNELING MAGNETIC RESISTANCE
28: WRITE X SELECTOR
29: READ X SELECTOR
31: WRITE WORD LINE
32: READ WORD LINE
34: REFERENCE BIT LINE
SAout
Vdd
Gnd
Vc
Vs
Vref
Is
Iref
Is+β
Iref+α
A
B
C
D
M1
M2
M3
M4
M5
M6
M7
M8
D1
D2
"0"
"1"
V
Fig. 17

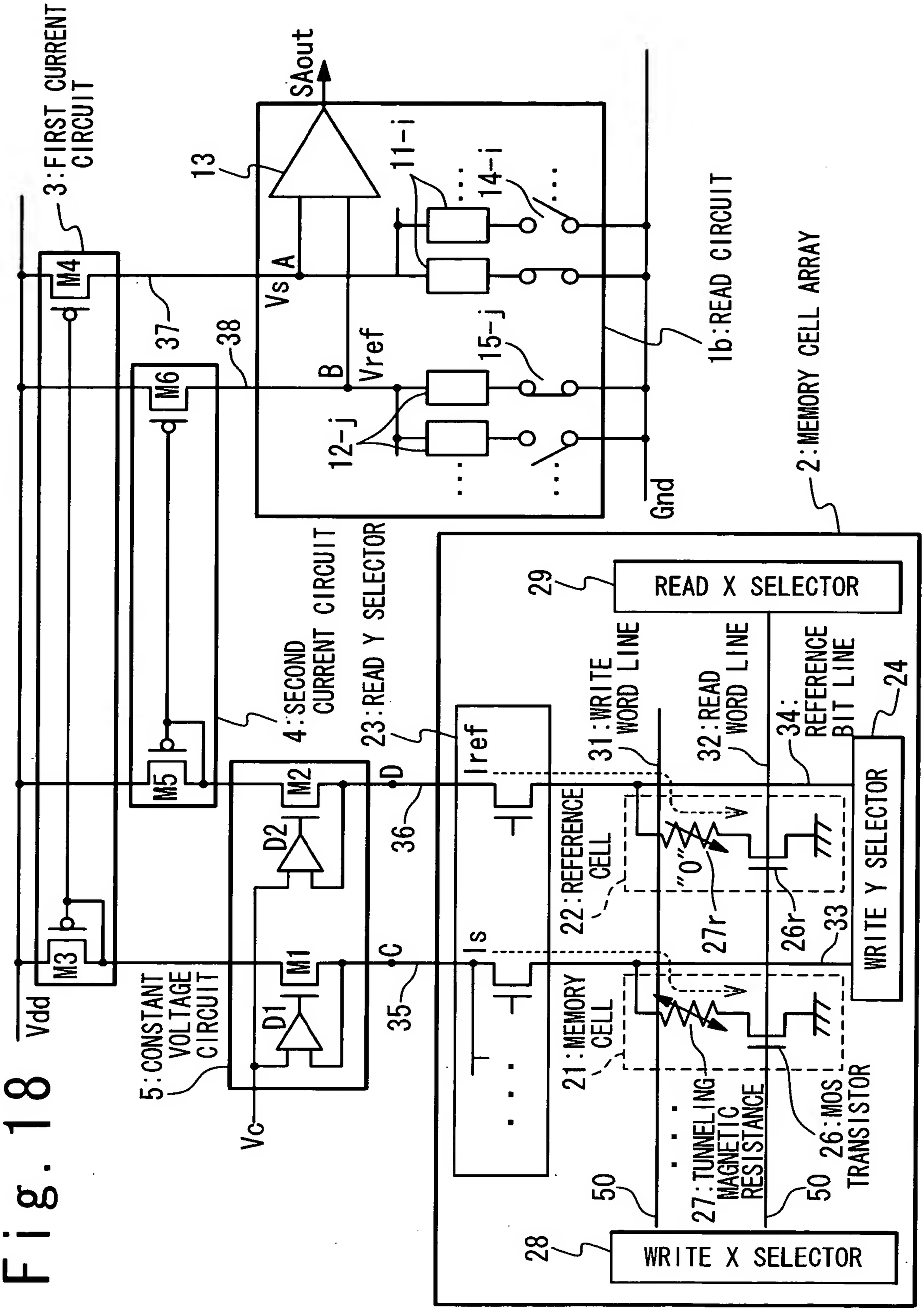

3:FIRST CURRENT CIRCUIT
SAout
13
11-i
14-i
Vs
A
B
Vref
12-j
15-j
Gnd
1b:READ CIRCUIT
2:MEMORY CELL ARRAY
M4
M6
M5
M2
M3
M1
37
38
36
35
C
D
Vdd
Vc
D2
D1
4:SECOND CURRENT CIRCUIT
5:CONSTANT VOLTAGE CIRCUIT
23:READ Y SELECTOR
Iref
Is
29
READ X SELECTOR
31:WRITE WORD LINE
32:READ WORD LINE
34: REFERENCE BIT LINE
24
22:REFERENCE CELL
21:MEMORY CELL
"0"
"1"
27r
26r
33
WRITE Y SELECTOR
27:TUNNELING MAGNETIC RESISTANCE
26:MOS TRANSISTOR
50
28
WRITE X SELECTOR

Fig. 18

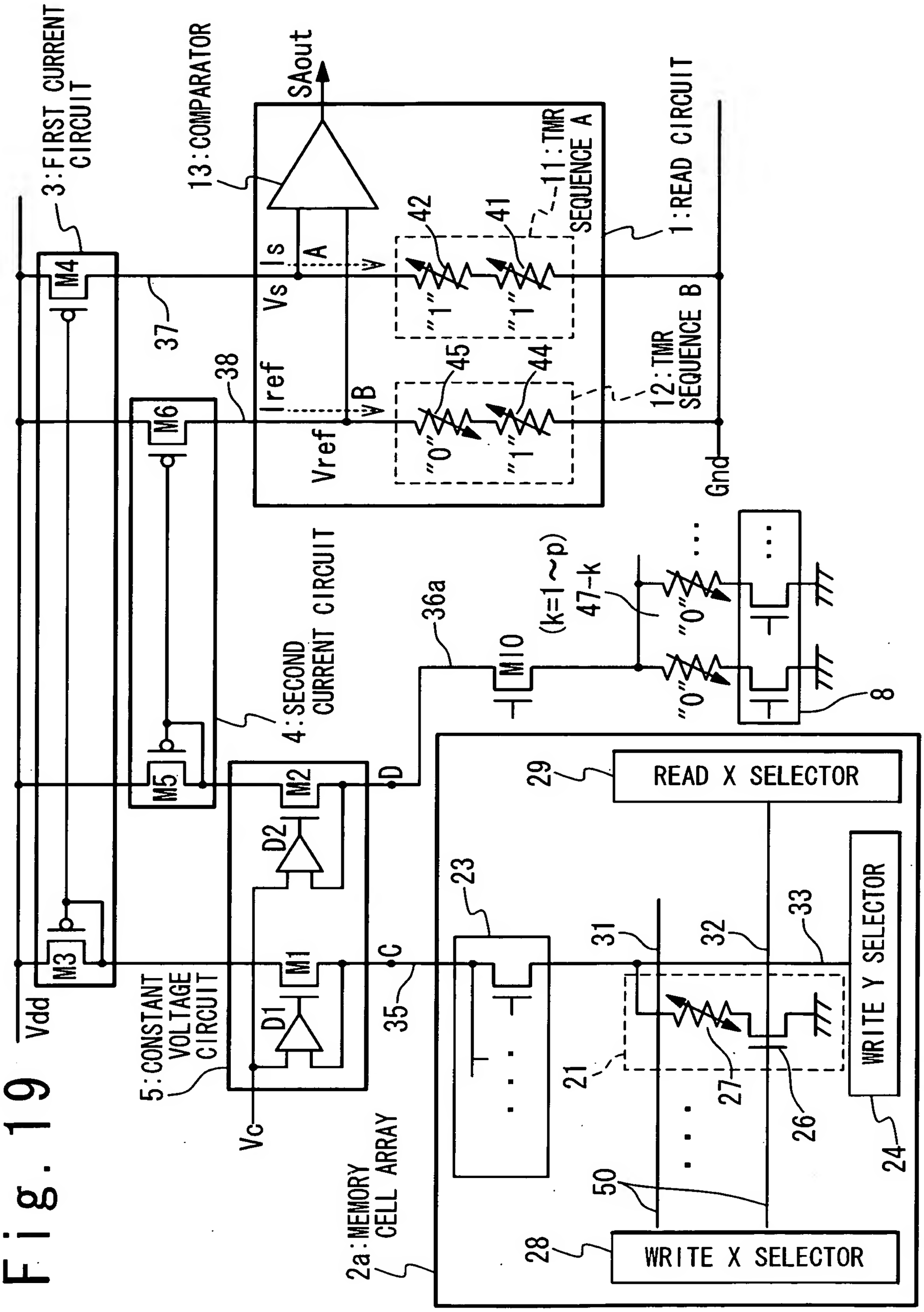

3:FIRST CURRENT CIRCUIT
13:COMPARATOR
SAout
11:TMR SEQUENCE A
1:READ CIRCUIT
12:TMR SEQUENCE B
Gnd
4:SECOND CURRENT CIRCUIT
36a
(k=1~p)
47-k
8
29
READ X SELECTOR
23
WRITE Y SELECTOR
5:CONSTANT VOLTAGE CIRCUIT
2a:MEMORY CELL ARRAY
WRITE X SELECTOR
Vdd
Vc
Vs
Is
Iref
Vref
A
B
C
D
37
38
35
31
32
33
21
27
26
24
50
28
42
41
45
44
M1
M2
M3
M4
M5
M6
M10
D1
D2

Fig. 19

Fig. 20

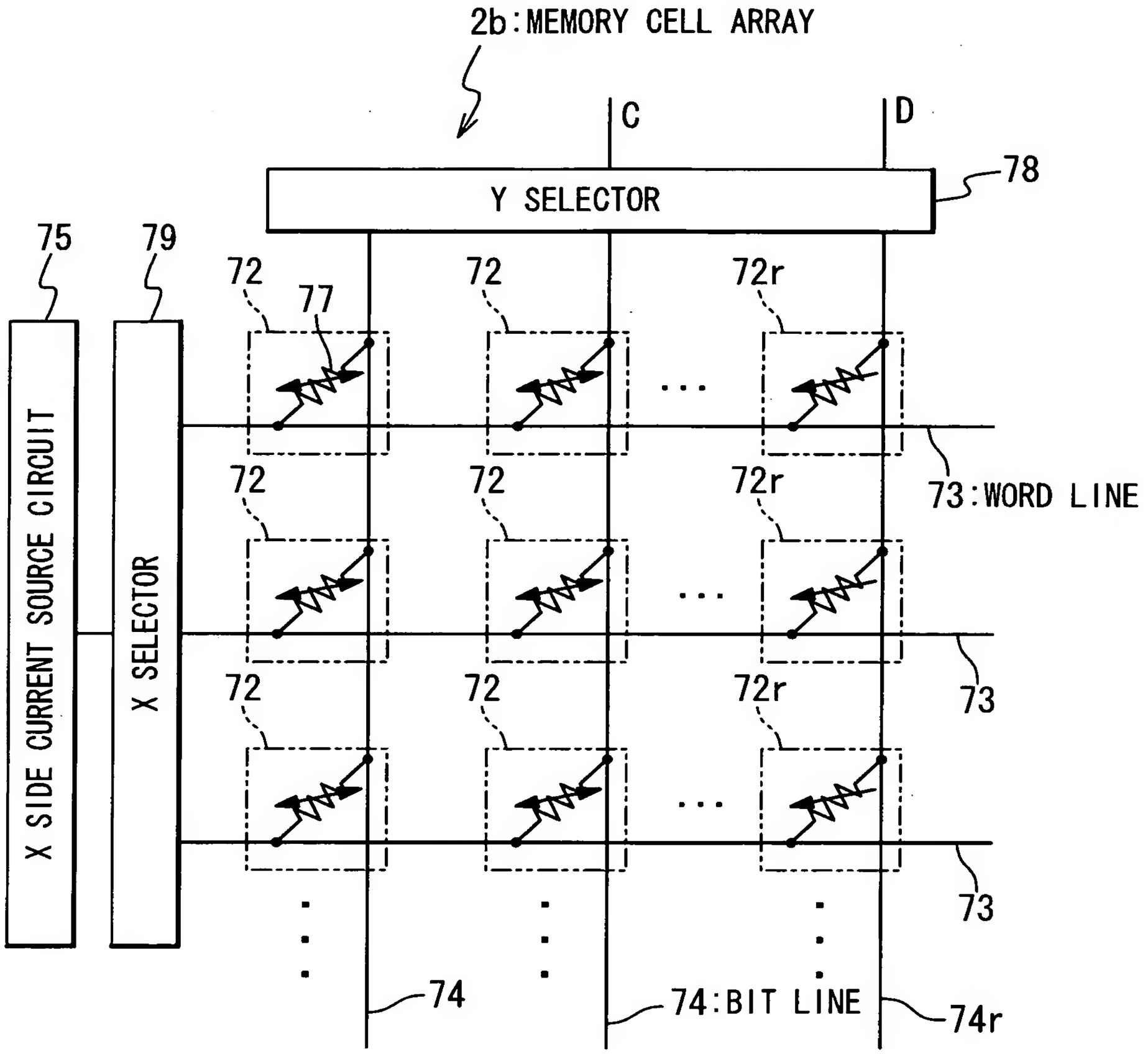
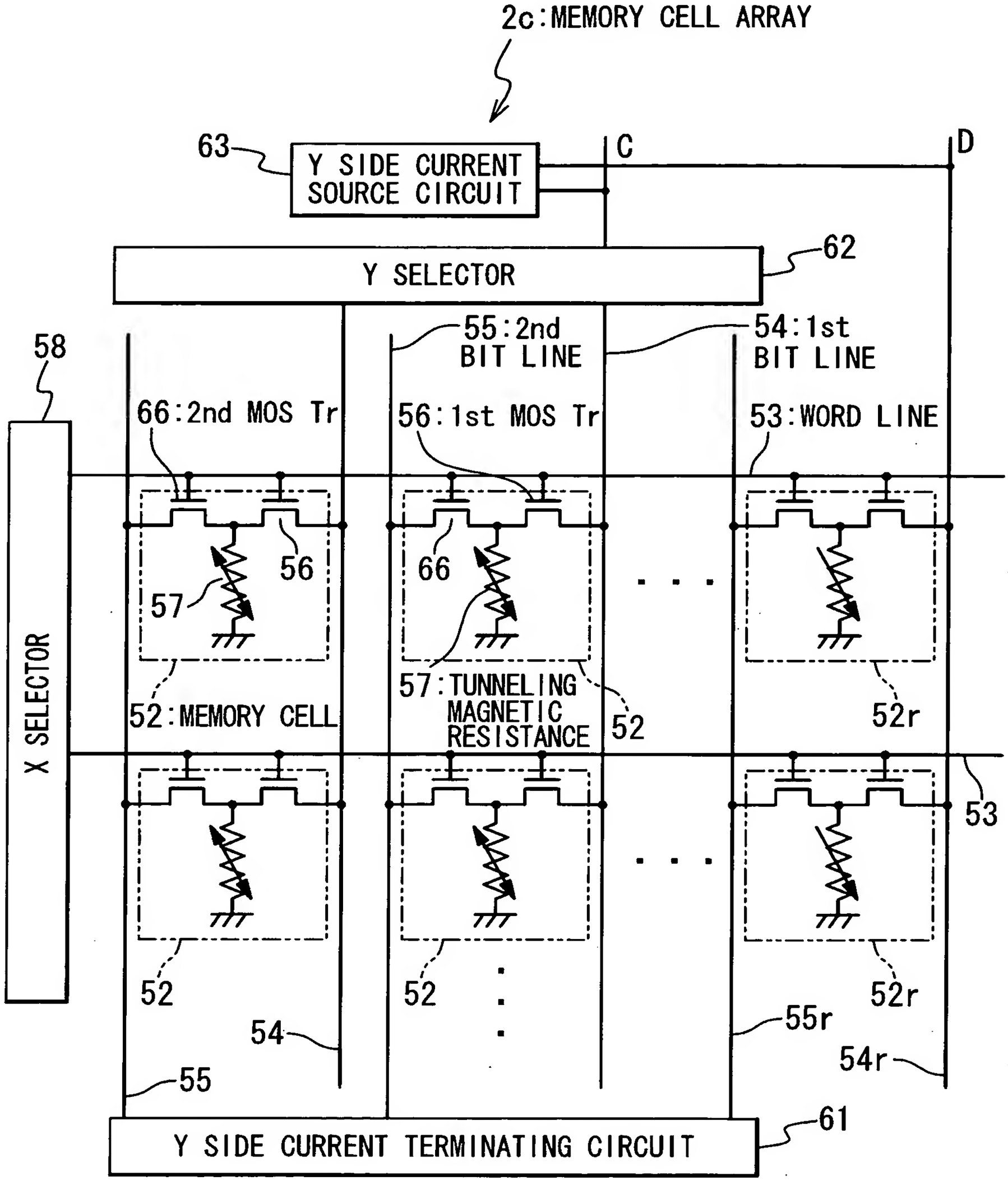

2b:MEMORY CELL ARRAY
C
D
78
Y SELECTOR
75
79
72
77
72r
X SIDE CURRENT SOURCE CIRCUIT
X SELECTOR
73:WORD LINE
73
74
74:BIT LINE
74r

Fig. 21


2c:MEMORY CELL ARRAY
63
Y SIDE CURRENT SOURCE CIRCUIT
C
D
62
Y SELECTOR
58
X SELECTOR
55:2nd BIT LINE
54:1st BIT LINE
66:2nd MOS Tr
56:1st MOS Tr
53:WORD LINE
56
57
66
52:MEMORY CELL
57:TUNNELING MAGNETIC RESISTANCE
52
52r
53
52
52
52r
54
55r
54r
55
61
Y SIDE CURRENT TERMINATING CIRCUIT